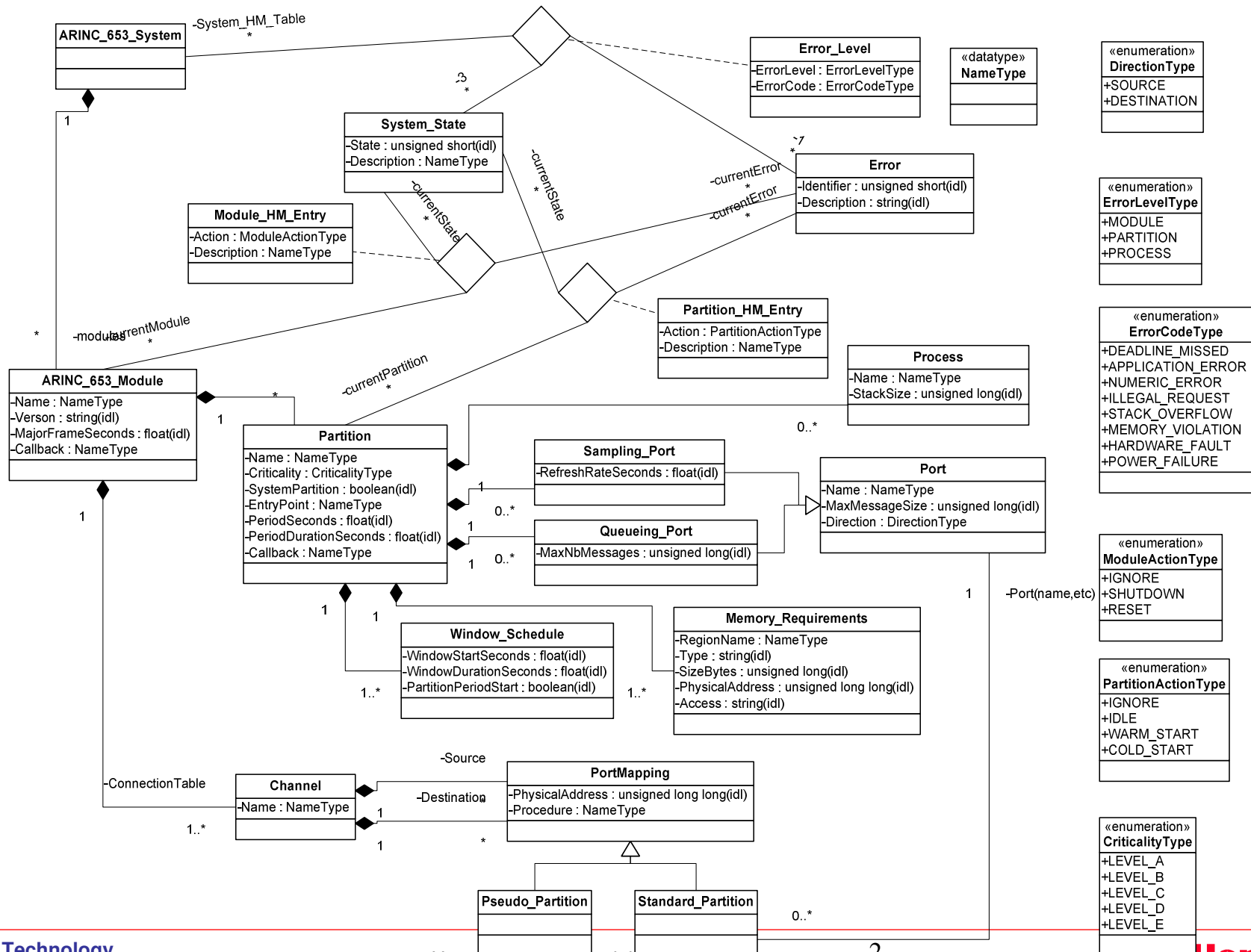


AADL to ARINC 653

Generating configuration details from a model

ARINC 653 Configuration



Direct Mappings

- Thread : Process
 - defining_thread_identifier : Name
 - Source_Stack_Size : StackSize
- Data port : Sampling Port
 - defining_port_identifier : PortName
 - Source_Data_Size : MaxMessageSize
 - direction : Direction
 - Compute_Execution_Time/
Compute_Deadline : Refresh_Rate_Seconds
- Event data port : Queuing Port
 - defining_port_identifier : PortName
 - Source_Data_Size / Queue_Size : MaxMessageSize
 - direction : Direction
 - Queue_Size : MaxNbMessages
- Connection : Channel
 - Source : source port
 - Destination : destination port

Partial Mapping

- Memory : Memory Requirements
 - Size depends on type
 - Mem Type & Access: AADL values are limited, but 653 values are unbounded
- Process : Partition
 - No Criticality or SystemPartition flag
- Port : Standard Partition
- Port : Pseudo Partition
 - Physical address calculation? No “Actual_Memory_Binding”

Generated Mappings

- Window Schedule
 - Generated completely from scheduling tools

- Health Monitoring (Error Annex)
 - System HM
 - Module HM
 - Partition HM
 - More than current Error Annex needed?
 - Doable by guidelines on the use of Error Annex features?

What's next

- Some clarifications needed in ARINC 653 spec
- Some new “standard” properties in AADL
- Health Monitoring Annex for AADL (partially covered in Error Annex).
 - Part of 653 Annex or generalized into standalone Annex?